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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,267	11/17/2003	Nathan R. Brown	2269-4375.1US (99-1029.01)	4590
24247	7590	06/08/2007	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			MACARTHUR, SYLVIA	
			ART UNIT	PAPER NUMBER
			1763	
			MAIL DATE	DELIVERY MODE
			06/08/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.



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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/715,267  
Filing Date: November 17, 2003  
Appellant(s): BROWN, NATHAN R.

**MAILED**  
**JUN 08 2007**  
**GROUP 1700**

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Brick G. Power  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed January 19, 2007 appealing from the Office action mailed April 5, 2006.

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**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

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The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

<u>Patent Number</u>	<u>Inventor Name</u>	<u>Publication Date</u>
6,623,343	Kajiware et al	9-2003
6,436,828	Chen et al	08-2002
6,594,542	Williams	07-2003
6,561,871	Sommer	05-2003

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

a) Claims 1 and 6-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Kajiware et al (US 6,623,343).

Kajiware et al teaches a system and method for CMP head having a multiple pressure annular zone subcarrier material removal control as illustrated in Figs. 8 and 9.

Regarding claims 1,6, and 10:Kajiware et al teaches providing a plurality of abutting concentric tubular pressure rings or bladders (pressurization structures) 255 such that a region is polished at different pressures than the surrounding regions. According to col. 18 lines 52-67 the pressurized gas or fluid (FBS1, FBS2, FB3, FBS4, FBS4, biasing the independently movable pressurization structures) are adjusted to provide the desired polishing profile across the wafer

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surface. The process of Kajiwara et al is directed to polishing at least one layer of the surface of the semiconductor device structure; hence it uses CMP as the polishing technique.

Regarding claims 7 and 8: Kajiwara et al teaches the use of both positive pressure (pressurized gas or fluid, see col.18 lines 60-65) and negative pressure (col.24 lines 1-10).

Regarding claim 9: CMP (chemical mechanical polishing) is taught in col.20 lines 17-37.

Regarding claim 11: The raised area is the basis of using different pressure along the wafer, this problem was observed by Kajiwara et al and discussed in col.2 lines 51-59.

Regarding claims 12,13, and 15: See col. 18 lines 52-67 and col. 20 lines 16-37 discuss applying pressure to the backside of the semiconductor.

Regarding claim 14: Kajiwara et al teaches the use of other wafers in the paragraph adjoining col. 24 and 25.

b) Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajiwara et al in view of Chen et al (US 6,436,828).

The teachings of Kajiwara et al were discussed above.

Kajiwara et al fails to teach the use of magnetic force to bias the wafer.

Chen teaches the use of magnetic force as a means to provide a downward force across the substrate.

The motivation to provide a magnetic force (in the form of magnetically sensitive particles) to bias the wafer magnetically is that this type of force is shown by Chen to provide enhanced control on the uniformity of force applied to the substrate, see col. 4

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lines 45-60. It is an alternative process of providing a pressure profile along the wafer than the using the positive or negative pressure source of Kajiwara et al as discussed in col. 1 lines 36-38. Thus, it would have been obvious for one of ordinary skill in the art at the time of the claimed invention to provide a magnetic force as the means to bias the wafer and provide a more optimal CMP result.

c) Claims 16-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sommer or Chen et al in view of Williams (US 6,594,542).

Sommer teaches a linear drive system for CMP.

The method of Sommer teaches selectively applying a plurality of different amounts of pressure to different, selected locations of a backside of the semiconductor device structure and a polishing or planarizing at least one layer of the surface of the semiconductor device structure, see the abstract and col. 15 lines 5-67. Sommer teaches at least one raised surface has been located and the adequate pressure applied to planarize see col. 16 lines 3-32. Note Sommer further teaches the use of magnets 420, 422, 424, and 426 in col. 12 lines 24-49, therein Sommer teaches downward F applied to the substrate can be varied as desired along the substrate by varying the distance between the magnets and polishing plate.

Recall Chen et al teaches CMP using magnetic force.

The method of Chen et al teaches selectively applying a plurality of different

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amounts of pressure to different, selected locations of a backside of the semiconductor device structure and a polishing or planarizing at least one layer of the surface of the semiconductor device structure, see abstract col. 6 lines 23-31.

Both Sommer and Chen et al fail to polishing a second semiconductor structure based on the applied pressure of the first.

Williams teaches a method and system for controlling CMP removal.

Col.6 teaches that after the completion of the polishing process, a thickness measurement is taken by metrology device 300. A second wafer is then polished using that data.

The motivation to modify the teachings of Sommer or Chen et al is to enhance the capabilities of the apparatus from the application of pressure to a specific wafer to wafers in an entire lot or batch. The combined teachings of Sommer or Chen et al and Williams will increase throughput. Thus, it would have been obvious for one of ordinary skill in the art at the time of the claimed invention to combine the teachings of Sommer or Chen et al with the teachings of Williams to polish a wafer, locate a raised area of the wafer and selectively apply pressure to the located raised are and polish a second wafer.

Regarding claims 26-28: Sommer teaches magnets are used according to col. 15 lines 47-67. Chen teaches the use of magnets to apply pressure in the abstract and the title of his patent.

#### **(10) Response to Argument**

- a) Kajiwara fails to anticipate the present invention

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Appellant argues that the bladders 255 of Kajiwara et al do not apply pressure to the surface of a semiconductor device structure. Applicant further argues that the membrane 250 of Kajiwara evens out the pressure along the backside the pressure applied.

The examiner notes that col. 18 lines 52-67 teaches that the use of the bladders 255 allows for pressure profile against the membrane and hence against the wafer 230, see lines 60 and 61. The claims do not exclude a membrane. Thus, the examiner maintains the rejection.

b) The Office has not established a prima facie case of obviousness with the combination of Kajiwara in view of Chen et al

Appellant argues that since the coils apply the magnet field against the membrane 104 the magnetic field is generated across the membrane and not the semiconductor. It is the examiner's position that the present invention does not exclude a membrane. It is noted that the magnetic field is against the membrane and hence against the wafer, see col. 4 lines 45-60 wherein Chen et al recites that a uniform magnetic field applied to the membrane will create a non-uniform pressure on the substrate.

Appellant further argues that the examiner has used hindsight reasoning to provide a motivation to combine the prior art of Kajiwara with Chen et al. In response to appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was



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made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Thus, the examiner maintains the rejection.

c) The Office has not established a prima facie case of obviousness with the combination of Sommer or Chen et al with Williams

Appellant argues that neither Sommer, Chen et al, nor Williams teach selectively applying pressure to raised area of a wafer. In response, the examiner reminds appellant the prior art of Sommer, Chen et al and Williams all teach using the process of CMP to polish a wafer and its layers (raised areas) disposed thereon. In col.1 lines 16-25, Sommer teaches that CMP achieves planarizing substrate surfaces (infers flattening raised features). Chen et al teaches that CMP is an acceptable method of planarizing (infers flattening raised features) substrate surfaces in col. 1 lines 9-30. The abstract of Williams teaches removing selected material (to include raised features) from a substrate surface.

Note Sommer further teaches the use of magnets 420,422, 424, and 426 in col. 12 lines 24-49, therein Sommer teaches downward F applied to the substrate can be varied as desired along the substrate by varying the distance between the magnets and polishing plate.

Recall Chen et al teaches CMP using magnetic force.

The method of Chen et al teaches selectively applying a plurality of different amounts of pressure to different, selected locations of a backside of the semiconductor device structure and a polishing or planarizing at least one layer of the surface of the semiconductor device structure, see abstract col. 6 lines 23-31.

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Both Sommer and Chen et al fail to polishing a second semiconductor structure based on the applied pressure of the first.

Williams teaches measuring the thickness of a wafer pre- and post-polishing in order to monitor and control the overall CMP process. In col. 6 lines 38-51, Williams teaches that the pressure applied by the wafer against the polishing surface is controlled during real-time. The measurements are used to ensure uniformity of polishing subsequent wafers. Thus, the examiner maintains the rejection.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



Primary Examiner Sylvia MacArthur

Conferees:

Gregory Mills

TQAS



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SPE

